CLAIMS

What is claimed is:

1. A method of forming a memory device having a self-aligned contact, comprising:

providing a substrate having a floating gate dielectric layer formed thereon;

forming a floating poly gate layer on the floating gate dielectric layer;

forming a silicon nitride layer on the floating poly gate layer;

forming a photoresist layer on the silicon nitride layer;

etching exposed areas of the silicon nitride layer and the floating poly gate layer using the photoresist layer as an etch mask;

forming an oxide layer over the exposed areas;

removing the photoresist layer and the silicon nitride layer to expose the floating poly gate layer;

forming poly spaces in the floating poly gate layer; and

depositing a silicon nitride layer over the poly spaces of the floating poly gate layer to form a self-aligned contact.

2. The method as set forth in claim 1, wherein the depositing of a silicon nitride layer comprises depositing a silicon nitride layer over the floating poly gate layer and the oxide layer.

3. The method as set forth in claim 1, and further comprising etching the silicon nitride layer to expose a portion of the floating poly gate layer.

4. The method as set forth in claim 1, and further comprising etching the silicon nitride layer to expose a portion of the floating gate dielectric layer.

5. The method as set forth in claim 3, further comprising etching the silicon nitride layer to create silicon nitride spacer formations.

6. The method as set forth in claim 5, wherein the silicon nitride spacer formations are formed over the floating poly gate layer.

7. The method as set forth in claim 1, wherein:

the floating poly gate layer is a first floating poly gate layer;

the method further comprises depositing a second floating poly gate layer over the first floating poly gate layer, the oxide layer, and the silicon nitride spacer formations.

8. The method as set forth in claim 7, further comprising depositing an interlayer dielectric on the second floating poly gate layer.

9. The method as set forth in claim 8, wherein the interlayer dielectric comprises an oxide/nitride/oxide stacked film.

10. The method as set forth in claim 3, wherein the etching of the silicon nitride layer comprises a dry etch process.

11. An apparatus formed using the method of claim 1.

12. An apparatus formed using the method of claim 5.

13. An apparatus formed using the method of claim 9.

14. A method of forming a memory device having a self-aligned contact, comprising:

providing a substrate having a floating poly gate feature and oxide features on source and drain sides of the floating poly gate feature;

forming poly spaces in the floating poly gate layer; and

depositing a silicon nitride layer over the poly spaces of the floating poly gate feature to form a self-aligned contact.

15. The method as set forth in claim 14, wherein:

the silicon nitride layer is deposited over the floating poly gate feature and the oxide features; and

the method further comprises etching the silicon nitride layer to expose a portion of the floating poly gate layer.

16. The method as set forth in claim 15, wherein the silicon nitride layer is etched into silicon nitride spacer formations.

17. The method as set forth in claim 16, wherein the etching of the silicon nitride layer results in formation of silicon nitride spacer formations over the floating poly gate layer.

18. The method as set forth in claim 16, wherein the method further comprises:

depositing a floating poly gate layer over the floating poly gate feature, the oxide features, and the silicon nitride spacer formations; and

depositing an interlayer dielectric on the floating poly gate layer.

19. The method as set forth in claim 16, wherein the etching of the silicon nitride layer comprises a wet etch process.

20. An apparatus formed using the method of claim 14.

21. An apparatus formed using the method of claim 16.

22. An apparatus formed using the method of claim 18.